MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

PDS0101 –INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

21 OCTOBER 2017
9.00 a.m. – 11.00 a.m.
(2 HOURS)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of **12 pages (including this page).**
2. Answer ALL FIVE questions.
3. Please **WRITE ALL YOUR ANSWERS IN THE QUESTION PAPER ITSELF** in the space allocated.

Question 1

(a) Explain the differences between analog domain and digital domain in term of:

(i) Signal
(ii) Noise response [2 marks]

(b) Given 2MByte of data at a rate of 20bps to transfer from device A to device B.
(i) Identify its period.
(ii) Identify the size of data in bits [Hint: Mega = 10^6 ; 1 byte = 8 bits]
(iii) Time needed to transfer all data in second (s) for:
- Serial transfer
- 20 bytes in parallel for each transfer

[1+1+1+1 marks]

Continued...

(c) Perform the arithmetics operation of (-40) – (-10) in 8-bit binary using the signed-2's complement representation for negative number(s). Show all steps.

[4 marks]

Question 2

(a) The state of 12-bit register is 110001111010_2. What is its context if it represents in:

(i) Decimal
(ii) Octal
(iii) Hexadecimal
Show all steps. [1+1+1 marks]

Continued...

(b) Given the Boolean function X = ABC + A'C + ABC':

(i) Draw the logic diagram of the given function.

(ii) Obtain the truth table of the function.

(iii) Simplify the function to a minimum number of literals using Boolean Algebra.

(iv) Obtain truth table of the function from the simplified expression and show that it is the same as the one in part (iii).

[2+2+1+2 marks]

Continued...

Question 3

(a) Given the function F(A,B), implement it using only NAND gates.

$$F(A,B) = (AB + A'B)$$

(i) Obtain the function F(A,B) using only NAND gates.

(ii) Draw the logic circuit using only NAND gates as expressed in (i)

[1+2 marks]

Continued...

(b) Design a combinational logic circuit with three inputs (A,B,C) and one output (X). The output is equal to logic 1 if A,B, and C less than 3_{10}, logic 0 otherwise.

(i) Obtain its truth table

(ii) Obtain its simplified Boolean function in POS form using K-Map

(iii) Draw the logic circuit based on the simplified Boolean function as in (ii)

(iv) Based on the simplified Boolean function in (ii), represent it using only NOR gates.

[2+2+2+1 marks]

Continued...

Question 4

(a) Use a block diagram to illustrate 3-bit parallel adder by using only full adder. Show how carries are connected between its next pair of bit.

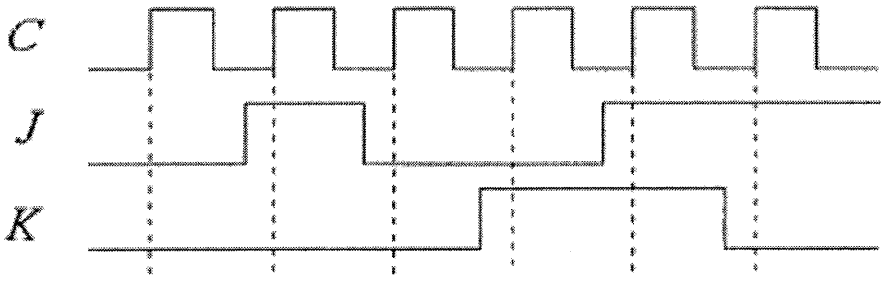
[2 Marks]

(b) Given the truth table for 2-4 line decoder (with enable input) as below. Draw the logic circuit for 2-4 line decoder. [3 marks]

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Continued...

(c) Determine the output Q in relation to positive-going transition clock (C) and its corresponding J-K inputs. Assume the flip-flop is initially RESET. [3 marks]



(d) Give TWO applications of flip-flops. [2 marks]

Continued...

Question 5

(a) Design a **3-bit synchronous counter** using **J-K flip-flops** that produce the following sequence: **000, 001, 010, 100, 101** and **repeat**. The undesired states must always go to DON'T CARE on the NEXT clock pulse. Your design should include

(i) State transition diagram showing all possible states,

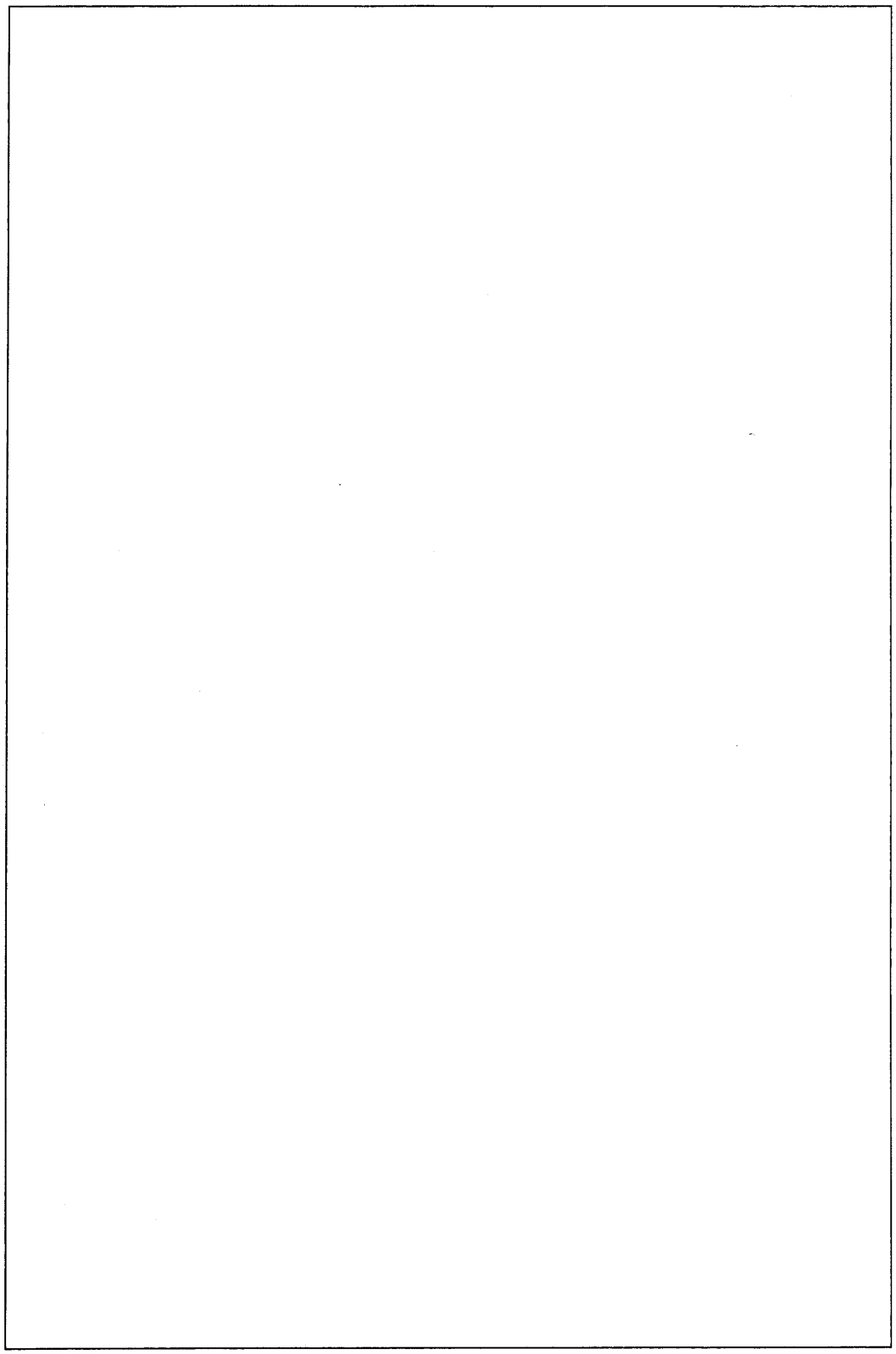
(ii) Circuit excitation table for J_A, J_B, J_C, K_A, K_B, K_C using Present States and Next States

(iii) Karnaugh Map simplification for each of J_A, J_B, J_C, K_A, K_B, K_C inputs.

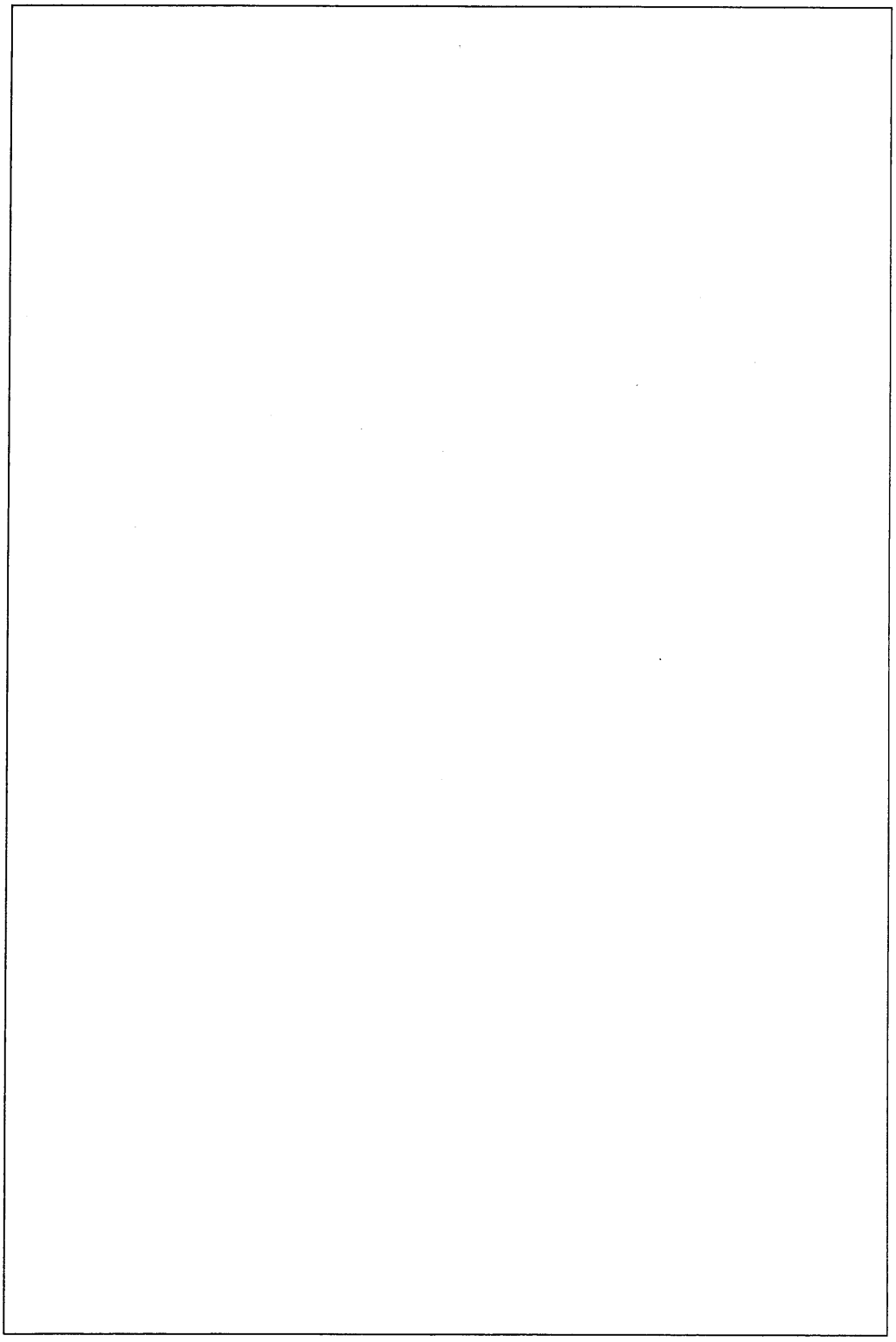
(iv) Draw the 3-bit synchronous counter using J-K flip-flops.

[1+2+3+2 marks]

Continued...

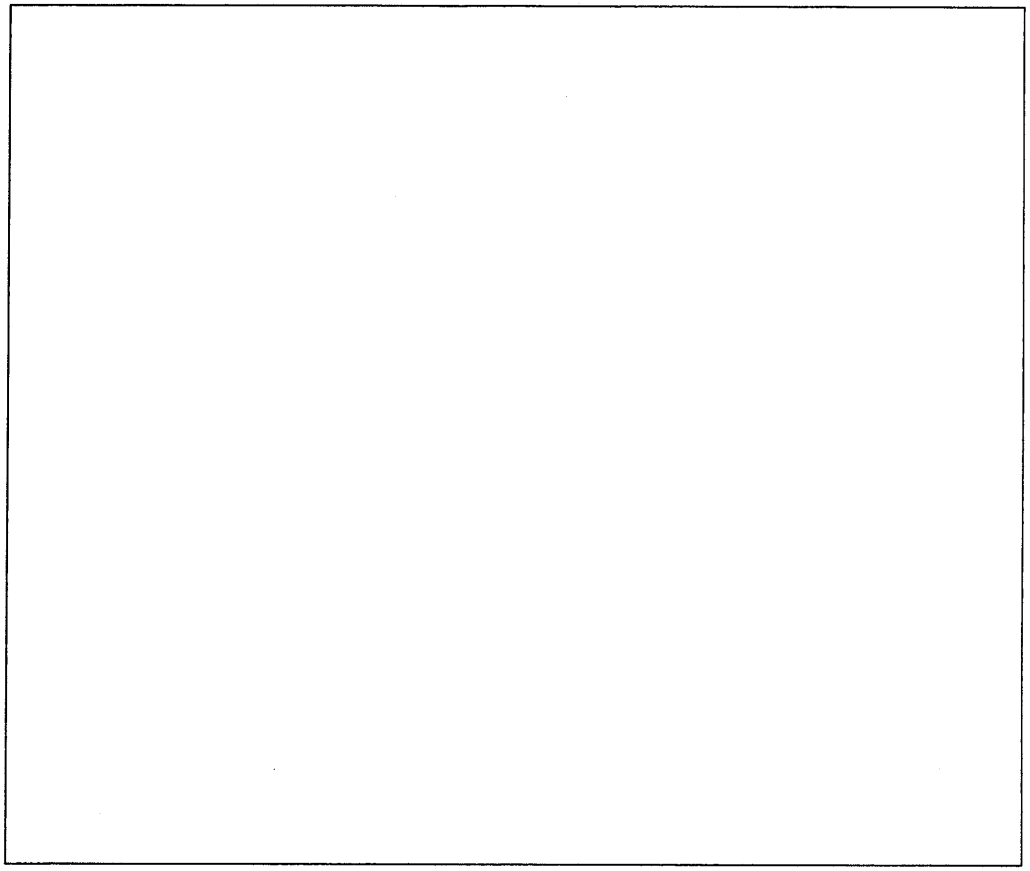


Continued...



Continued...

(b) Draw a 4-bit parallel-in parallel-out block register. [2 marks]



End of Paper